Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A shift register circuit provided with a plurality of register blocks each having a flip-flop that operates in synchronization with a clock signal and a transfer gate for controlling the clock signal supplied to the flip-flop,

the plurality of register blocks being serially connected together, and

an input control signal of the transfer gate of a corresponding register block being brought into an ON-state only in a specified period during which an output of the flip-flop of the corresponding register block changes.

Claim 2 (original): A shift register circuit as claimed in claim 1, wherein

when a level of an input signal inputted to each register block and a level of an output signal outputted from the register block differ from each other, the transfer gate of the register block is brought into the ON-state.

Claim 3 (original): A shift register circuit as claimed in claim 1, wherein

the flip-flop is a D-type flip-flop, and

the register block has a logic operation section for executing a logic operation of an input signal of the register block and an output signal of the register block and controls the transfer gate to be turned on and off based on a signal representing a logic operation result of the logic operation section.

Claim 4 (original): A shift register circuit as claimed in claim 1, wherein

the flip-flop is an SR-type flip-flop,

the transfer gate is comprised of a first transfer gate for controlling input of the clock signal inputted to a set terminal of the SR-type flip-flop and a second transfer gate for controlling input of the clock signal inputted to a reset terminal of the SR-type flip-flop, and

the register block has a first logic operation section and a second logic operation section for executing a logic operation of an input signal of the register block and an output signal of the register block, controls the first transfer gate to be turned on and off based on a signal that represents a logic operation result of the first logic operation section and controls the second transfer gate to be turned on and off based on a signal that represents a logic operation result of the second logic operation section.

Claim 5 (original): A shift register circuit as claimed in claim 1, wherein

the register block has a retainment signal circuit that inputs to a clock input terminal of the flip-flop of the register block a retainment signal for bringing the output of the flip-flop into a retained state in a period during which the transfer gate is in an OFF-state.

Claim 6 (original): An image display device comprising a plurality of pixels arranged in a matrix form, a plurality of data signal lines for supplying image data to be written into the plurality of pixels, a plurality of scanning signal lines for controlling the image data to be written into the pixels, a data signal line drive circuit for driving the data signal lines and a scanning signal line drive circuit for driving the scanning signal lines, wherein

at least one of the data signal line drive circuit and the scanning signal line drive circuit includes the shift register circuit claimed in claim 1.

Claim 7 (original): An image display device as claimed in claim 6, wherein

an output pulse width of the data signal line drive circuit is controlled by controlling a pulse width of an input signal inputted to the register block of the first stage of the shift register circuit.

Claim 8 (original): An image display device as claimed in claim 7, wherein

a side black region is displayed on an upper side and a lower side of an image display screen by writing a black signal into all the data signal lines while increasing the pulse width of the input signal inputted to the register block of the first stage of the shift register circuit so that all the data signal lines are brought into an active state by the data signal line drive circuit.

Claim 9 (original): An image display device as claimed in claim 6, wherein

at least one of the data signal line drive circuit and the scanning signal line drive circuit is formed on a substrate identical to that of the plurality of pixels.

Claim 10 (original): An image display device as claimed in claim 9, wherein

an active element constituting at least the data signal line drive circuit is provided by a polysilicon thin film transistor.

Claim 11 (original): An image display device as claimed in claim 10, wherein

the active element is formed on a glass substrate through a process at a temperature of not higher than 600°C.

Claim 12 (original): A shift register circuit as claimed in claim 1, wherein

the clock signal has a level lower than a clock signal input level of the flip-flop,

the register block has a level shift circuit for shifting a level of the clock signal so that the level of the clock signal becomes not lower than the clock signal input level of the flip-flop, and

the level shift circuit is brought into an operating state every register block only in a specified period during which the output of the flip-flop changes.

Claim 13 (original): A shift register circuit as claimed in claim 12, wherein

when a level of an input signal inputted to each register block and a level of an output signal outputted from the register block differ from each other, the transfer gate of the register block is brought into the ON-state, and

when a level of an input signal inputted to each register block and a level of an output signal outputted from the register block differ from each other, the level shift circuit of the register block is brought into an operating state.

Claim 14 (original): A shift register circuit as claimed in claim 12, wherein

the register block has a retainment signal circuit that inputs to a clock input terminal of the flip-flop of the register block a retainment signal for bringing the output of the flip-flop into a retained state in a period during which the transfer gate is in an OFF-state.

Claim 15 (original): A shift register circuit as claimed in claim 14, wherein

the register block has an OFF-state signal circuit that inputs to the clock input terminal of the level shift circuit an OFF-state signal of a level at which no current flows through the level shift circuit in the period during which the transfer gate is in the OFF-state.

Claim 16 (original): A shift register circuit as claimed in claim 14, wherein

the level shift circuit is connected to a power source line and a ground line, and

the register block has a disconnecting circuit for disconnecting either one of the power source line and the ground line of the level shift circuit in the period during which the transfer gate is in the OFF-state.

Claim 17 (original): A shift register circuit as claimed in claim 12, wherein

the flip-flop is a D-type flip-flop, and

the register block has a logic operation section for executing a logic operation of an input signal and an output signal of the register block and controls the transfer gate to be turned on and off based on a signal representing a logic operation result of the logic operation section.

Claim 18 (original): A shift register circuit as claimed in claim 12, wherein

the flip-flop is an SR-type flip-flop,

the transfer gate is comprised of a first transfer gate for controlling the input of the clock signal inputted to a set terminal of the SR-type flip-flop and a second transfer gate for controlling the input of the clock signal inputted to a reset terminal of the SR-type flip-flop, and

the register block has a first logic operation section and a second logic operation section for executing a logic operation of an input signal and an output signal of the register block, controls the first transfer gate to be turned on and off based on a signal that represents a logic operation result of the first logic operation section and controls the second transfer gate to be turned on and off based on a signal that represents a logic operation result of the second logic operation section.

Claim 19 (original): An image display device comprising a plurality of pixels arranged in a matrix form, a plurality of data signal lines for supplying image data to be written into the pixels, a plurality of scanning signal lines for controlling the image data to be written into the pixels, a data signal line drive circuit for driving the data signal lines and a scanning signal line drive circuit for driving the scanning signal lines,

at least one of the data signal line drive circuit and the scanning signal line drive circuit includes the shift register circuit claimed in claim 12.

Claim 20 (original): An image display device as claimed in claim 19, wherein

an output pulse width of the data signal line drive circuit is controlled by controlling a pulse width of an input signal inputted to the register block of the first stage of the shift register circuit.

Claim 21 (original): An image display device as claimed in claim 19, wherein

a side black region is displayed on an upper side and a lower side of an image display screen by writing a black signal into all the data signal lines while increasing the pulse width of the input signal inputted to the register block of the first stage of the shift register circuit so that all the data signal lines are brought into an active state by the data signal line drive circuit.

Claim 22 (original): An image display device as claimed in claim 19, wherein

at least one of the data signal line drive circuit and the scanning signal line drive circuit is formed on a substrate identical to that of the pixels.

Claim 23 (original): An image display device as claimed in claim 22, wherein

an active element constituting at least the data signal line drive circuit is provided by a polysilicon thin film transistor.

Claim 24 (original): An image display device as claimed in claim 23, wherein

the active element is formed on a glass substrate through a process at a temperature of not higher than 600°C.

Claim 25 (currently amended): A shift register circuit comprising a plurality of register blocks each having a flip-flop that operates in synchronization with a clock signal and a transfer gate for controlling the clock signal supplied to the flip-flop,

the plurality of register blocks being serially connected together, and further comprising:

a control circuit outputting a control signal to each of the transfer gates, the control signal being input into ~~so as to bring~~ the transfer gate of a corresponding register block such that the control signal is brought into an ON-state only when an output signal of the flip-flop of the corresponding register block changes.